COST EFFECTIVE EDGE MACHINING OF SILICON WAFERS TO MINIMISE THE POLISHING PROCESS

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Introduction

The current move to 300mm silicon wafer technology presents new technical challenges at all stages of the integrated circuit fabrication process. The quality of prime wafers is of great importance, and here we describe recent work at Cranfield on an edge grinding process with the potential to dramatically reduce the need for subsequent edge polishing and etching in prime wafer production.

Wafer edge quality must be of the highest order to withstand damage from handling. Any chipping of the edge, no matter how small, will contaminate the process and could cause irreversible damage to the integrated circuitry during subsequent fabrication stages. Rapid Thermal Processing (RTP) can also cause pre-existing microscopic cracks from the grinding process to propagate as the wafer rapidly undergoes large temperature changes during deposition stages; sometimes resulting in total wafer breakage.

Generically speaking, current silicon wafer edge processing begins with fixed abrasive grinding using metal bonded diamond wheels to rough grind the diameter, orientation flat or notch, to the required size and edge form. This process produces a surface roughness of between 300 to 400nm RMS with 20μm, or more, sub-surface microcrack damage. Etching and free abrasive edge polishing is then used to remove the damaged layer, producing 2 to 5 nm RMS surface roughness. Since etching and polishing are time consuming, costly and have negative environmental implications, wafer manufacturers are looking for ways to reduce or eliminate these two processes. Whatever the solution, it should satisfy the goals of higher yield and lower cost.

Based on these requirements, and previous work at Cranfield which investigated the “ductile regime” grinding of brittle materials [1], a machine and process have been developed to edge grind 200mm and 300mm silicon wafers.

Machine Configuration

The Cranfield Precision Silicon Wafer Edge Grinder has been designed with the aid of finite element analysis to create a machine with high stiffness to weight ratio and good damping of parasitic structural vibrational modes. These characteristics are required to control the interaction between wheel and workpiece to a level compatible with high quality, low damage grinding.

Three air bearing spindles are mounted horizontally on the machine; workhead spindle, O/D grinding spindle and high speed notch grinding spindle. The O/D and notch grinding wheel spindles are mounted opposite to, and on either side of the workhead axis. Both are configured to feed in a radial direction, towards the workhead axis.

Wafers are transferred from the load station by robot handler and placed on an automated inspection station. Each wafer is centered, the orientation mark (notch or flat) located, and then transferred to the workhead vacuum chuck. The wafer’s outside diameter is ground in a plunge mode using grooved peripheral O/D wheels (the wheel grooves having been previously formed on the machine to the required wafer edge profile). From the standoff position, a rapid search feedrate is used until an acoustic touch sensor detects contact between wheel and workpiece. Only then is a change to the slower grinding feedrate triggered, thus helping to reduce overall cycle time.

The same grooved O/D wheels are used to grind the orientation flat. A 4mm diameter wheel is used to grind the notch, and is grooved in the same manner as the O/D wheels. The wheel groove diameter is made small enough to allow generation of the required notch bottom radius. Either orientation flat or notch are ground in a contour creep feed mode, with the workhead and grinding wheel axes slaved together by CNC, in order to generate the required geometrical form.

After grinding, the wafer is returned to the inspection station where edge profile form accuracy and centering are measured, together with notch or orientation flat geometry.

Wheel conditioning and geometrical control of the cross-sectional edge profile is maintained through the use of a periodic in-situ wheel re-forming process. The forming interval is determined by the degradation in wafer edge profile, and quality of surface finish.

The Grinding Process

The O/D grinding process can be broken down into discrete grinding stages, from roughing to final finishing. The number of stages used depends upon the amount of material to be removed and quality of surface to be obtained. For the purposes of this paper, we shall look at a 3-stage process.

A typical three stage grinding process for incoming wafers with a square edge profile would be as follows:

1) Rough grind: Using a large grit size, the wafer is ground to approximately 0.3mm oversize on diameter. This stage is used for major stock removal and, generates a near net shape edge profile from the incoming wafer’s square edges.

2) Semi-finish grind: Using an intermediate grit size, a further 0.2mm of material is removed from the diameter. This stage is intended to remove material efficiently,
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without creating significant sub-surface damage, whilst at the same time further refining the edge profile to minimise uneven wear on the finish grinding wheel.

3) Finish grind: Using a small grit size, approximately 0.1 mm of material is removed on diameter to bring the wafer to target size, and generate the final surface.

Each of the three grinding stages produces a progressively smoother surface with consequently less sub-surface damage.

Results

Surface quality has been measured in terms of surface roughness and sub-surface damage. Surface roughness has been measured using the Rank Taylor Hobson Form Talysurf (Gaussian filter, 12 x 0.08 mm cutoffs).

Sub-surface damage (SSD) in the form of micro-cracks has been assessed by Cranfield University using polishing and etching techniques. A small segment of wafer is taken and mounted vertically in resin. The sample is lapped and polished so as to generate a flat (chord) on the wafer edge. An etch is used to reveal any micro-cracks which are then measured using an optical microscope. This method of polishing a chord along the wafer edge, serves to magnify any sub-surface microcracks by typically up to 30x for ease of observation. With knowledge of the original wafer diameter and the polished chord length, the true damage depth (perpendicular to the wafer edge) can be calculated.

Figures 1 to 3 show the sub-surface damage revealed by this technique for each of the three O/D grinding stages. One can clearly see the micro-cracks produced during rough and semi-finish grind (fig.1, & fig.2, respectively).

Figure 4, shows the relationship between sub-surface damage and surface roughness for a number of samples. The spread of roughness values was created by using a range of feedrates for each stage. Surface roughness for typical process feedrates is ~750 nm RMS (roughing), ~200 nm RMS (semi-finishing), and ~20-80 nm RMS (finishing). As expected, the general trend is for increased sub-surface damage with increased roughness. Minimum sub-surface damage observed for the finish stage is typically <2 μm.

Using the 3-stage O/D process, and including notch or flat grinding, cassette-to-cassette cycle times of approximately 180 seconds and 270 seconds have been achieved for 200 mm and 300 mm wafers respectively.
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![Figure 1: Micrograph of SSD produced by ROUGH grinding](image1)

![Figure 2: Micrograph of SSD produced by SEMI-FINISH grinding](image2)

![Figure 3: Micrograph of SSD produced by FINISH grinding](image3)

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![Figure 4: Relationship between SSD and surface roughness](image4)

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Conclusions

The process described above, when implemented on the Cranfield Precision Silicon Wafer Edge Grinder, is capable of producing a high quality ground surface of 20-80 nm RMS with typically <2 μm sub-surface damage, with a reasonable throughput. This improved ground surface quality helps to reduce the requirement for further etching and polishing stages, thereby giving the potential for cost savings and a more environmentally compatible prime wafer fabrication process.

References


[2] SSD assessments were performed by Dr. Sue Impey & Mr A. Dyer, School of Industrial and Manufacturing Science, Cranfield University, U.K.

Ductile to brittle transition investigated by plunge-cut experiments in monocrystalline silicon

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1 Introduction

We have derived experimental data on the ductile to brittle transition from well defined cutting experiments using an inclined plunge-cut method [1] with continuously increasing uncut chip thickness (fig.1).

![Fig. 1: Principle of plunge-cut experiments.](image)

The plunge-cut experiments were performed on a Moore M18 Aspheric Generator at a constant cutting speed of 20 mm/min. We used four different diamond tools with nose radii of 6 mm and 0.76 mm and rake angles of 0° and -45°, respectively. The samples were diamond turned with a surface finish < 3 nm rms. The selected cutting directions were <100> on a {100}-surface and <221> on a {111}-surface. The crystallographic orientation was determined from Laue diagrams. In order to assure reproducibility, each plunge-cut was repeated three times.